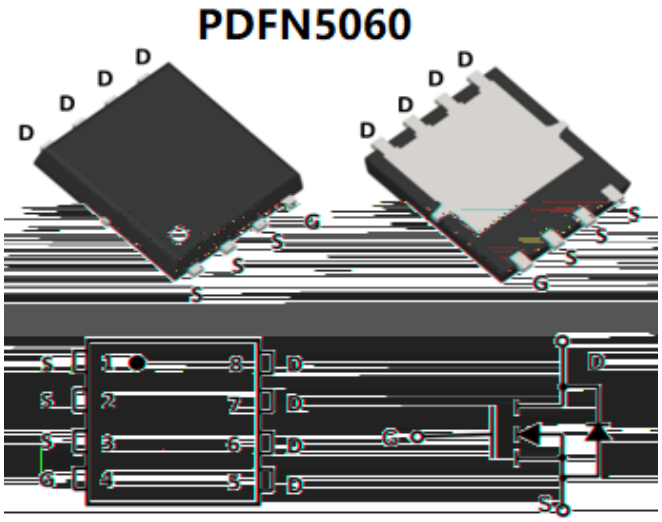
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 100V
- I_D 120A
- $R_{DS(ON)}$(at V_{GS}=10V) 4.2mohm
- 100% UIS Tested
- 100% V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- Power switching application
- Uninterruptible power supply
- PD charge
- DC-DC convertor

■ Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_C=25	I_D	120	A
	Tc=100		76	
Pulsed Drain Current [A]		I_{DM}	480	A
Avalanche energy [B]		EAS	552	mJ
Total Power Dissipation [C]	Tc=25	P_D	108	W
	Tc=100		43	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	Steady-State	$R_{\theta JA}$	45	55	/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.95	1.16	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG120G10BR	F1	G120G10BR	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= 20V, V_{DS}=0V	-	-	100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	2	2.8	4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=60A	-	3.5	4.2	mΩ
		V_{GS}=10V, I_D=20A	-	3.5	4.2	mΩ
Diode Forward Voltage	V_{SD}	I_S=60A,V_{GS}=0V	-	0.9	1.2	V
Gate resistance	R_G	f=1MHz, Open drain	-	0.8	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	120	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHZ	-	4400		pF
Output Capacitance	C_{oss}		-	1600		
Reverse Transfer Capacitance	C_{rss}		-	20		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=60A	-	39	-	nC
Gate-Source Charge	Q_{gs}		-	14	-	
Gate-Drain Charge	Q_{gd}		-	6	-	
Reverse Recovery Chrage	Q_{rr}	I_F=60A, di/dt=500A/us	-	180	-	nC
Reverse Recovery Time	t_{rr}		-	40	-	nS
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V,I_D=60A R_{GEN}=2.2Ω	-	20	-	nS
Turn-on Rise Time	t_r		-	95	-	
Turn-off Delay Time	$t_{D(off)}$		-	30	-	
Turn-off fall Time	t_f		-	7	-	

A. Repetitive rating; pulse width limited by max. junction temperature.
B. T_J=25 , V_{DD}=50V, V_G=10V, R_G=25Ω, L=2mH, IAS=23.5A.
C. P_d is based on max. junction temperature, using junction-case thermal resistance.
D. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25 . The maximum allowed junction temperature of 150 . The value in any given application depends on the user's specific board design.

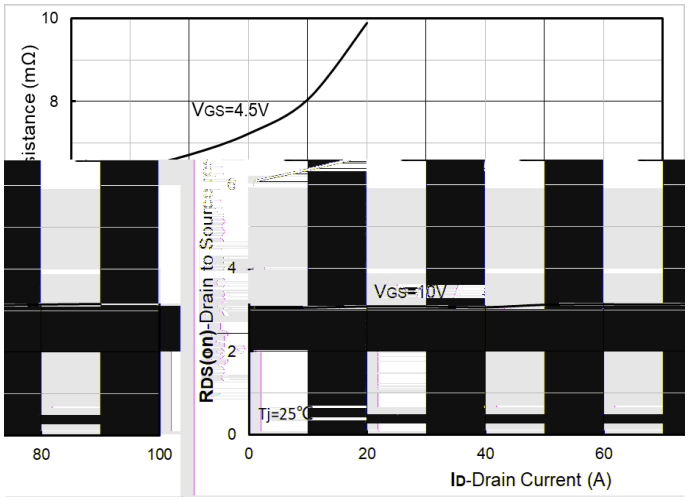


Figure7. RDson VS Drain Current

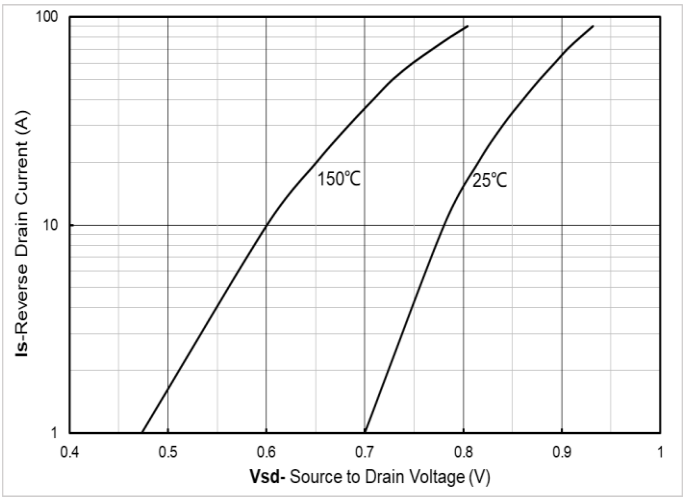


Figure8. Forward characteristics of reverse diode

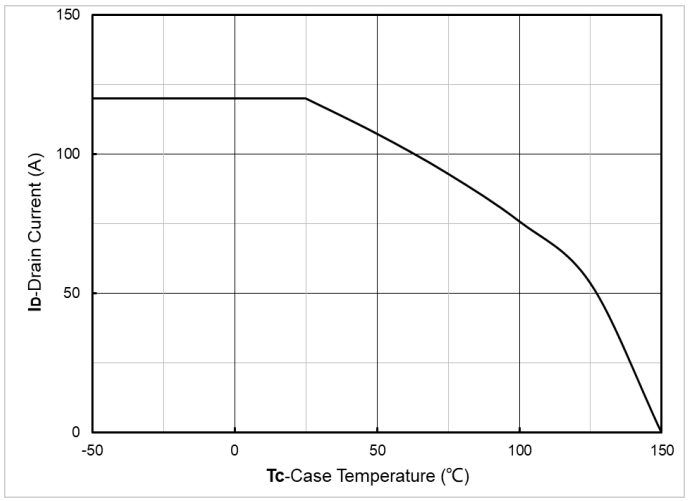


Figure9. Current dissipation

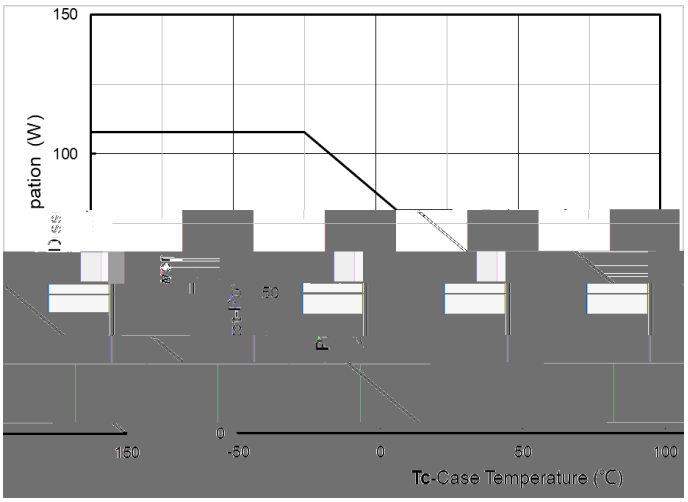


Figure10. Power dissipation

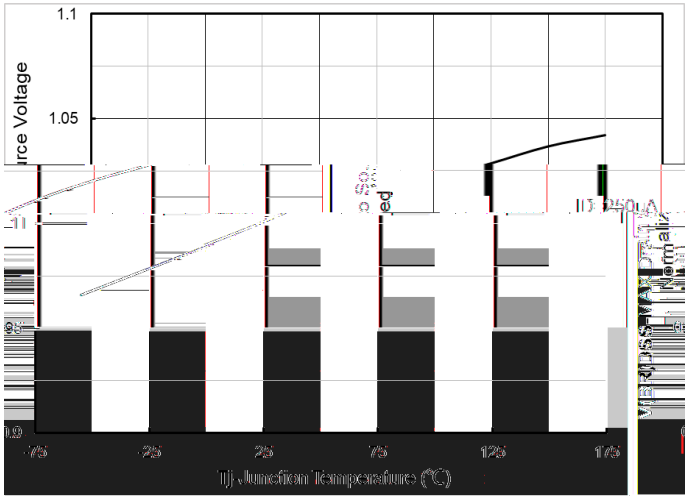


Figure11. Normalized breakdown voltage

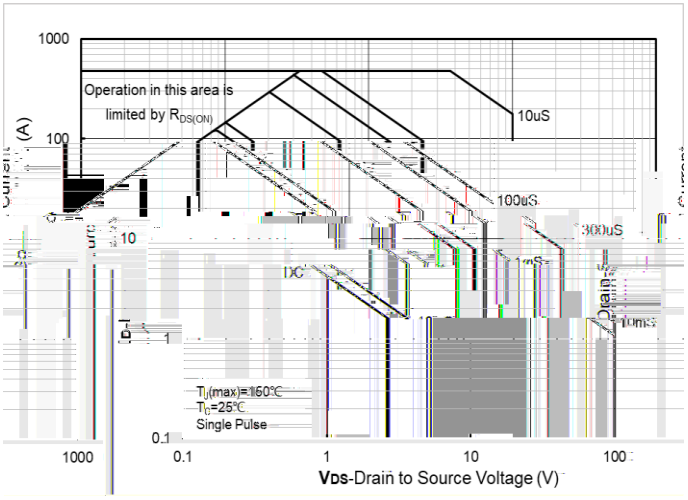


Figure12. Safe Operation Area

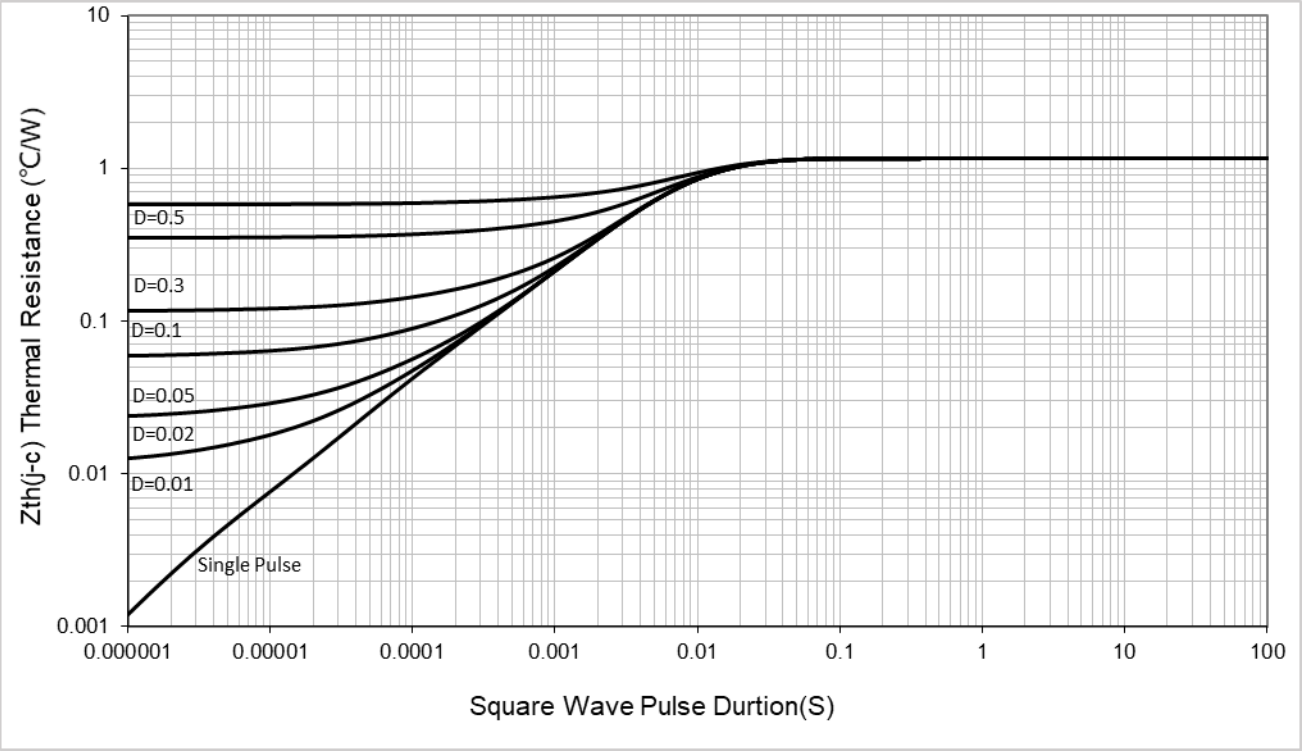
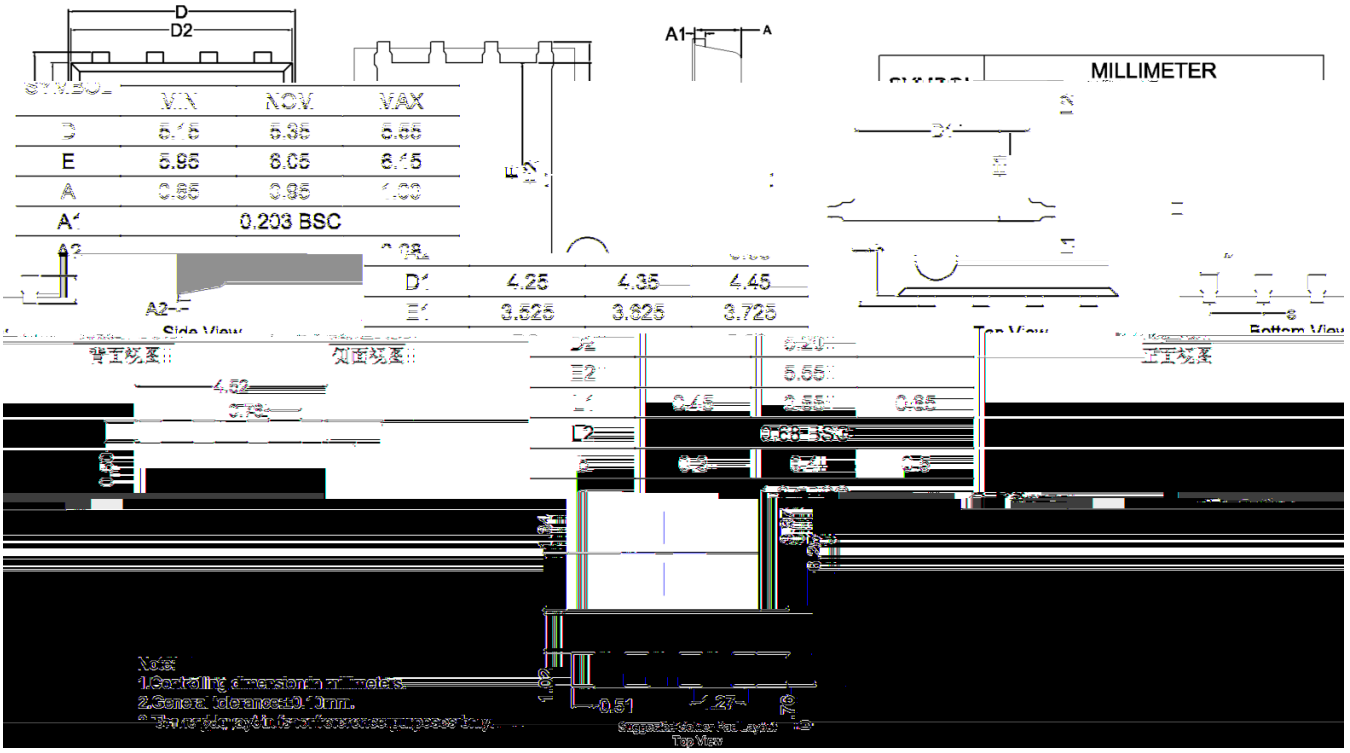


Figure13. Maximum Transient Thermal Impedan

■ PDFN5060-8L-D-0.95MM Package information



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